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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/609,567	06/30/2000	Robert D. Bateman	042390.P9220	2886

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Kenneth M Seddon
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
7th Floor
Los Angeles, CA 90025

EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	14

DATE MAILED: 12/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/609,567	Applicant(s) BATEMAN, ROBERT D.	
	Examiner Tuan V. Thai	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed September 29, 2003. This amendment has been entered and carefully considered. Claims 1-22 remain pending in the application.

2. Applicant's arguments with respect to claims 1-22 have been considered but are deemed to be moot in view of the new grounds of rejection. The finality of the previous office action is hereby withdrawn. Any inconvenience is *SINCERELY* regretted.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American

Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-19 are rejected under 35 U.S.C. § 102(e) as being anticipated by Robertson et al. (USPN: 5,956,744); hereinafter Robertson.

As per claim 1; Robertson teaches the invention as claimed including a method for storing data in a cache comprising prioritizing locked way of the cache higher than a recently used way (e.g. see column 22, line 33 bridging column 23, line 10); specifically, starting at lines 34 et seq., Robertson clearly discloses it is beneficial to ensure the cache entries expected to be used most often would not be replaced ***even if they are the least recently used by employing the priority lock level PL[1:0]*** wherein the locked priority is the highest priority (even if it is not the least recently used entry/way; e.g. see lines 53-54).

As per claim 2, storing data in the least recently used way (e.g. see column 6, lines 12 et seq.; column 22, lines 48-50);

As per claim 3, Robertson discloses prioritizing the locked

way higher than a least recently used way and storing data in the least recently used way (e.g. see column 22, line 33 bridging column 23, line 10);

As per claim 4, locking at least one way/entry of the cache to provide the locked way (e.g. see column 22, lines 54 et seq.);

As per claims 5 and 8, the further limitation of reading/writing data from/to **a** way (entry) of the cache prior to prioritizing the locked way wherein the way being the recently used way is embedded in the system of Robertson since (a) Robertson, in fact, discloses the concept of prioritizing the locked way to be the highest priority level even though the way being the least recently used way (e.g. see arguments with respect to claim 1); in addition (b) data from cache is always being accessed (read/write) regardless of before or after the prioritizing operation in order to carry out the prioritizing/lock operation;

As per claims 6-7, Robertson discloses setting a bit in the parameter section 420, PL[1:0] bit, to indicate the prioritizing of the locked way, the way could be least-recently-used way (e.g. see column 21, lines 28-29; column 22, lines 63 et seq., figure 6); Robertson further discloses the priority level for each cache entry/way may be stored in a cache priority look-up table (register as being claimed) (e.g. see column 6, lines 19-20);

As per claims 9-10, the further limitation of locking the

first way of the cache, and locking the second way of the cache to provide an additional lock way is taught by Robertson as plurality of cache ways/entries being locked (e.g. see column 33, lines 66-67); and prioritizing the locked way higher than the additional locked way is equivalent to the different priority level can be applied to the individual cache entries for carrying-out the lock (e.g. see column 33, lines 27 et seq.);

As per claims 11-12, setting the first, second, third bits of the register to indicate priority of the locked/additional-locked/LRU way is taught by Robert as setting a bit in the parameter section 420 for each cache entries, PL[1:0] bit, to indicate the prioritizing of the locked way, the way could be least-recently-used way (e.g. see column 21, lines 28-29; column 22, lines 63 et seq., figure 6);

As per claim 13, Robertson discloses locking a first way/entry of a cache (table 4 on column 22, when PL[1:0] status at [1:1]; also see line 54 et seq. on the same column); accessing a second/third way of the cache is taught as other cache entries of the six entries of cache 305 are accessed for data (cache 305 is full (e.g. see column 22, lines 20-26), prioritizing the first way of the cache higher than the second way of the cache is equivalent taught as locked way/entry having highest priority (e.g. see column 22, lines 53-54), and writing the data to the second way of the cache is embedded in Robertson's system; for

example, Robertson discloses low priority cache entry/way is discarded for writing the miss data to the same way/entry before a high priority level cache entry/way (locked way) (e.g. see column 22, lines 50-51);

As per claim 14; Robertson discloses setting a bit in the parameter section 420, PL[1:0] bit, to indicate the prioritizing of the locked way, the way could be least-recently-used way (e.g. see column 21, lines 28-29; column 22, lines 63 et seq., figure 6); Robertson further discloses the priority level for each cache entry/way may be stored in a cache priority look-up table (register as being claimed) (e.g. see column 6, lines 19-20);

As per claims 15-16; the further limitation of writing data into the second way occurs if the second way has been more recently access than the first/third way is taught by Robertson; for example, as known in the memory storage art and being disclosed by Robertson, caches generally flush and replace the cache entry least recently used which become more recently accessed (e.g. see column 22, lines 28-29); in addition, if the cache entries expected to be used most often would not be replaced (e.g. see column 22, lines 35-36);

As per claim 17; Robertson discloses the invention as claimed including an apparatus comprises a cache (cache 305, figure 5) having multiple ways/entries including first and second ways (e.g. see column 22, line 20); a circuit (memory cache

configuration cache service unit 17) for write data to the first way if the first way has been accessed more recently than the second way is taught by Robertson; for example, as known in the memory storage art and being disclosed by Robertson, caches generally flush and replace the cache entry least recently used which become more recently accessed (e.g. see column 22, lines 28-29); in addition, if the cache entries expected to be used most often would not be replaced (e.g. see column 22, lines 35-36);

As per claims 18-19, the further limitation of locking the second way and a memory location for indicating the priority of the cache ways/entries including the first and second way is taught by Robertson to the extent that it is being claimed, for example, setting a bit in the parameter section 420, PL[1:0] bit, to indicate the prioritizing of the locked way, the way could be least-recently-used way (e.g. see column 21, lines 28-29; column 22, lines 63 et seq., figure 6); Robertson further discloses the priority level for each cache entry/way may be stored in a cache priority look-up table (register as being claimed) (e.g. see column 6, lines 19-20).

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (USPN: 5,956,744); hereinafter Robertson.

As per claims 20-22 Robertson discloses the invention as claimed, detailed above with respect to claims 1-19. Robertson, however does not particularly disclose a computer-readable medium having of instructions to carry out the steps and apparatus of claims 1-19 to be implemented on a computer as being claimed in claims 20-22. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, cd-rom, etc.) carrying computer-executable instructions for implementing a method, because it would facilitate the transporting and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a cd-rom from which Windows can be installed onto other systems, which is a lot

easier that running a long cable or hand typing the software onto another system. The examiner takes Official Notice of this teaching. Therefore, it would have been obvious to put Robertson's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Robertson's program on other systems.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is 703-305-3842.

The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays or e-mailed at ***tuan.thai@uspto.gov;***
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew M. Kim can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Serial Number: 09/609,567

Art Unit: 2186

TVT/November 25, 2003

Tuan V. Thai

PRIMARY EXAMINER

Group 2100